

Proven Cyrix®
quality and
technology
that you can
rely on

VIA Cyrix® III processor

The VIA Cyrix® III processor is based on the socket 370 bus interfaced to a high-performance core. Features include 64KB L1 cache, 256KB L2 cache, a 133MHz Front Side Bus, a dual issue floating point unit, MMX™ technology and 3DNow!™ instructions.

The VIA Cyrix® III processor is superscalar with separate pipelines that allow two instruction streams to be processed at the same time. Each pipeline is seven stages deep to allow the processing of many instructions per clock cycle.

It also features a large, two level translation buffer (TLB) and a 512 entry branch target

buffer (BTB) for faster branch translation and branch prediction. Advanced architectural techniques also include register renaming for out-of-order execution, handling of data dependencies between pipelines through data forwarding and bypassing, and speculative execution after a predicted branch.

These design innovations deliver optimum performance while running Microsoft Windows® 2000, Windows® 98, Windows® 95, Windows® NT, OS/2, DOS, UNIX®, Solaris®, Linux and all other x86 operating systems.

Architectural Features	Cyrix® III	Pentium® III	Celeron™
133 FSB Support	X	X	
Advanced 3D Instructions	X	X	
Superscalar	X	X	X
Superpipelined	X	X	X
Register Renaming	X	X	X
80-bit FPU	X	X	X
Out-of-Order Completion	X	X	X
Speculative Execution	X	X	X
Multi-Branch Prediction	X	X	X
Data Dependency Removal	X	X	X
L1 Cache	64k (Unified)	16k+16k	16k+16k
L2 Cache	256k Full Speed	512k Half Speed	128k Full Speed



For a full technical report, visit www.viatech.com

Sales Offices Information

Contact one of these VIA offices for information on VIA Cyrix® processors:

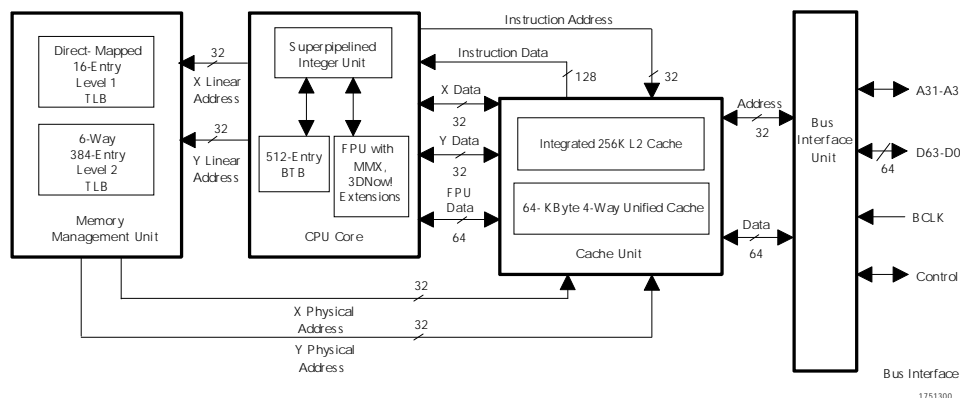
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VIA Cyrix® III



Technical Specifications

Clocking	2.5x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x flexible bus/core clock ratios
Compatibility	Compatible with MMX™ and 3DNow! technology; supports all x86 operating systems including Windows® 95, 98 and NT, Linux, OS/2®, DOS, Solaris, UNIX® and others
Bus	64-bit external data bus, 32-bit pipelined address bus; supports 66,100 and 133 FSB.
Voltage	2.2V core, GTL+ I/O
Pin/Socket	Socket 370
Floating Point	Dual issue, 80-bit, x87 FP instructions, MMX, and 3DNow!
Cache	64k L1 and 256k L2 running at core speed

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